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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,163	08/20/2003	Deborah A. Hagen	SC12699TK	5785
23125	7590	06/14/2005	EXAMINER	
FREESCALE SEMICONDUCTOR, INC. LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02 AUSTIN, TX 78729			COLEMAN, WILLIAM D	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/644,163

Applicant(s)

HAGEN, DEBORAH A.

Examiner

W. David Coleman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 09 July 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 and 16-20 is/are rejected.
- 7) ☒ Claim(s) 14 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date various.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

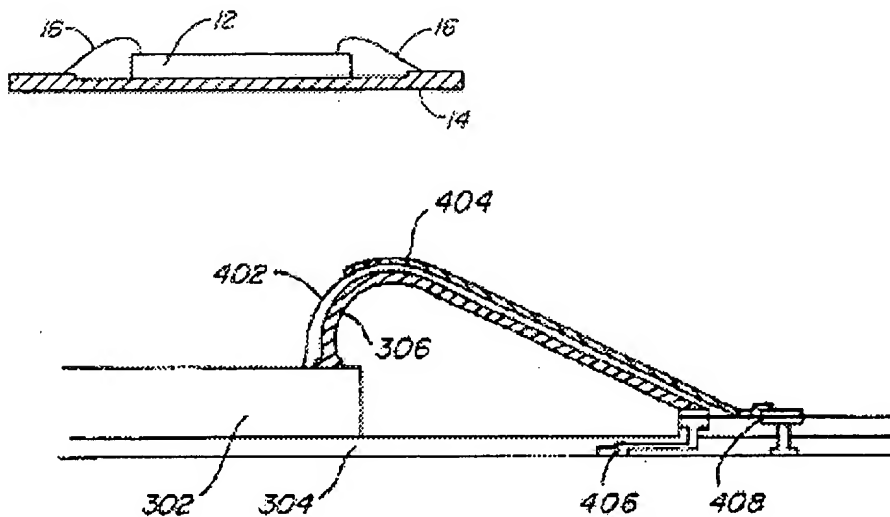
1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-14 and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Beatson et al., U.S. Patent 6,608,390 B2.

Beatson discloses a system and a method of fabricating a system as claimed. See FIGS. 1A-4B, where Beatson discloses the following limitations.



3. Pertaining to claim 1, Beatson teaches a system, comprising:  
a circuit portion, containing more than electrical conductors; and

a wirebonded assemblage, overlying the circuit portion, wherein the wirebonded assemblage comprises a plurality of wirebonded wires, wherein each of the plurality of wirebonded wires are electrically coupled, and wherein the wirebonded assemblage provides electrical shielding for the circuit portion.

4. Pertaining to claim 2, Beatson teaches a system as in claim 1, wherein the circuit portion comprises at least one of an active component and a passive component (the Examiner takes the position that the semiconductor die is the active component and the wirebonds are the passive components which can behave as inductors or capacitors).

5. Pertaining to claim 3, Beatson teaches a system as in claim 1, wherein the circuit portion comprises at least a portion of an integrated circuit.

6. Pertaining to claim 4, Beatson teaches a system as in claim I, wherein the plurality of wirebonded wires comprise at least five wirebonded wires.

7. Pertaining to claim 5, Beatson teaches a system as in claim 1, wherein the circuit portion has a non-linear geometry (see **FIG. 4B** where the conductive layer **404** is not the same dimension as conductive layer **306**).

8. Pertaining to claim 6, Beatson teaches a system as in claim I, wherein the circuit portion is located in a cavity of a substrate (see **FIG. 1A**).

9. Pertaining to claim 7, Beatson teaches a system as in claim 1, wherein the wirebonded assemblage provides heat spreading for the circuit portion (please note that the extra conductive film will also function as a heat spreader).

10. Pertaining to claim 8, Beatson teaches a system as in claim 1, wherein at least one of the plurality of wirebonded wires is coupled to a predetermined voltage level.

11. Pertaining to claim 9, Beatson teaches a system as in claim 8, wherein the predetermined voltage level is approximately ground (column 2, line 31).

12. Pertaining to claim 10, Beatson teaches a system as in claim 1, further comprising: a second circuit portion, overlying the wirebonded assemblage.

13. Pertaining to claim 11, Beatson teaches a system as in claim 10, wherein the second circuit portion is electrically coupled to the wirebonded assemblage.

14. Pertaining to claim 12, Beatson teaches a system as in claim 1, wherein at least one of the plurality of wirebonded wires is not wirebonded to the circuit portion.

15. Pertaining to claim 13, Beatson teaches a system as in claim 1, further comprising:

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a second plurality of wirebonded wires electrically coupled to the circuit portion for communicating electrical signals.

16. Pertaining to claim 15, Beatson teaches a system as in claim 1, further comprising:  
a conductive layer underlying the circuit portion, wherein the conductive layer is electrically coupled to the wirebonded assemblage to encapsulate the circuit portion.

17. Pertaining to claim 19, Beatson teaches a system, comprising:  
a circuit portion, containing more than electrical conductors;  
a first wirebonded wire, overlying any two edges of the circuit portion; and  
a second wirebonded wire, overlying any two edges of the circuit portion;  
wherein the first wirebonded wire and the second wirebonded wire are electrically coupled, and  
wherein the first wirebonded wire and the second wirebonded wire are used to provide electrical shielding for the circuit portion.

18. Pertaining to claim 20, Beatson teaches a system as in claim 19, wherein the circuit portion comprises an integrated circuit.

*Claim Rejections - 35 USC § 103*

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

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having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

20. Claims 14 and 16-18 are rejected under 35 U.S.C. 103(a) as being obvious over Gehman et al., U.S. Patent Publication No. US 2004/0195591 A1.

21. The applied reference has a common Assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2). It would have been obvious to one of ordinary skill in the art to increase the integration density of the system by stacking the dies having shielding on top of one another.

### *Objections*

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22. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

*Conclusion*

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856.

The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



W. David Coleman  
Primary Examiner  
Art Unit 2823

WDC